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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,275	09/18/2006	Fukashi Morishita	050099-0355	8498

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EXAMINER	
LOXAS, PETER J	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,275	MORISHITA ET AL.	
	Examiner	Art Unit	
	PETER LOXAS	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/23/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, and 5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see page 8, lines 5-6, filed 10/23/2009, with respect to the rejection(s) of claim(s) 1 under 35 U.S.C. § 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chen et al. US Patent No. 5,767,549. Chen et al. show a MOS structure that provides charge accumulation below the channel of the MOS.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (Chang) US Patent no. 5,912,842, Adan, US Patent No. 6,204,534 B1, and further in view of Chen et al. (Chen) US Patent No. 5,767,549.

RE CLAIM 1: Chang teaches (Fig. 4) **a semiconductor memory device comprising: a plurality of memory cells** (40, col. 4, line 51) **arranged in a matrix; and a gate line** (CG, col. 5, line 10), **a word line** (WL, col. 5, line 8), **a bit line** (BL) **and**

a source line (CS, col. 5, line 11)**, wherein each of said plurality of memory cells** (40) **includes:**

Chang teaches the limitation of claim 1 as shown above. Chang is silent as to the components of the memory cell.

However, in an analogous structure, Adan teaches **a transistor** (T2) **having a first impurity region** (9) **and a second impurity diffusion region** (5) **opposed to each other through a first channel formation region** (7)**, a first gate electrode** (4a) **formed above said first channel** (7) **formation region** (4a)**, and a charge accumulation node** (commonly known in the art, (e.g. Chang (col. 1, lines 45-51)**; and a transistor** (T2) **connected to said storage transistor** (T1) **in series, having said first impurity diffusion region** (9)**, a third impurity diffusion region** (6) **opposed to said first impurity diffusion region** (9) **through a second channel formation region** (8)**, and a second gate electrode** (4b) **formed above said second channel formation region** (8)**, said second impurity diffusion region** (5) **is connected to said source line** (Source)**, said third impurity diffusion region** (6) **is connected to said bit line** (Drain)**, said first gate electrode** (4a) **is connected to said gate line** (commonly know in the art, e.g. Chang, fig. 4, 40(0,0))**, and said second gate electrode** (4b) **is connected to said word line** (commonly known in the art e.g. Chang, fig. 4, 40(0,0))**,**

and by turning on/off said access transistor, a potential of said first impurity diffusion region is switched to a fixed potential or a floating state, to thereby control the potential of said charge accumulation node,

and a threshold voltage of said storage transistor is thereby set at high level or low level. (The performance properties of the device during operation do not distinguish the claimed devices over the prior art. See MPEP 2112).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the inventions of Chang and Adan in order to provide a nonvolatile memory array (col. 4, line 49-50) to a memory device.

Chang and Adan show substantially the limitations of claim 1 as shown above. Chang and Adan are silent as to the charge accumulation node is formed below the first channel formation region.

However, in an analogous structure, Chen teaches **a charge accumulation node formed below channel formation region** (abstract).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ a charge accumulation below the channel, as shown by Chen, in order to overcome the problem of a floating gate (abstract).

RE CLAIM 2: Claim 2 is considered to be a product-by-process claim. Therefore, the limitation, "**threshold voltage of said storage transistor is set at high level by raising a potential of said first gate electrode to high level from low level, with said access transistor turned on, and said threshold voltage of said storage transistor is set at low level, by raising the potential of said first gate electrode to high level from low level, with said access transistor turned off**", does

not carry any patentable weight the claim drawn to a structure, because a distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

RE CLAIM 3: Adan teaches **an SOI substrate** (abstract) **in which a semiconductor substrate** (1, col. 5, line 2)**, an insulating layer** (2, buried oxide, col. 5, line 2)**, and a semiconductor layer** (3, Si layer, col. 5, line 4) **are laminated in this order, wherein said first to third impurity diffusion regions** (9, 5, 6) **and said first and second channel formation regions** (8, 7) **are respectively formed in said semiconductor layer** (3)**.**

Adan shows the limitations of claim 3 as shown above. Adan is silent as to the charge accumulation node.

However, in an analogous structure, Chang teaches **the charge accumulation node is constituted as a part of said semiconductor layer** (Chang states, "hot electrons induced BCBT are injected into the floating gate 22. The resultant accumulation of charge…, col. 1, line 46-48)**.**

It would have been obvious to a person of ordinary skill in the art at the time the invention was made employ a charge accumulation node as shown by Chang in order to increase the threshold voltage to operate as an enhancement mode device (col. 1, line 52).

RE CLAIM 5: Chang teaches a **first memory cell** (40(0,0), fig. 6, col. 6, line 8) **in which said threshold voltage of said storage transistor (STr) is set at high level** (see MPEP 2112)**; a first reference bit line** (Chang recites, "during reading operations, the sense amplifier associated with the selected bit line is enabled for determining the voltage on the selected bit line." Chang is silent as to the first bit line connected to the first memory cell. However, it would have been obvious to a person of ordinary skill in the art.) **connected to said first memory cell** (40(0,0))**;**
a second memory cell (40(1,0), col. 6, line 42) **in which said threshold voltage of said storage transistor** (40a) **is set at low level** (see MPEP 2112)**;**
a second reference bit line (same as lines 3-6 above) **connected to said second memory cell** (40(1,0))**; and**
a sense amplifier circuit (Chang recites, "the array 70 further includes sense amplifiers, col. 5, lines 16-17)

that compares each potential of said first and second reference bit lines and the potential of the bit line connected to a reading memory cell serving as a reading object, and thereby detects whether said threshold voltage of said storage transistor provided in said reading memory cell (Chang recites, "during reading operations, the sense amplifier associated with the selected bit line is enabled for determining the voltage on the selected bit line") **is set at high level or low level** (see MPEP 2112).

RE CLAIM 6: Chang teaches (fig. 6) the **storage transistor** (40a, floating gate, col. 5, line 33)**, said access transistor** (40b, select transistor, col. 4, line 14)**, a first transistor** (82(0), col. 12, line 8)**, and a second transistor** (82(1), col. 6, line 10) **are sequentially connected in series from a power supply potential** (V_{CC}) **side, between said power supply potential** (V_{CC}) **and a ground potential, and each gate of said first and second transistors** (82(0) and 82(1)) **is connected to a drain of said first transistor** (82(0))**.**

RE CLAIM 7: Claim 7 is considered to be a product-by-process claim. Therefore, the limitation, "**when said threshold voltage of said storage transistor provided in a writing memory cell serving as a writing object is set at high level, the potential of low level is applied to a bit line connected to said writing memory cell, and when said threshold voltage of said storage transistor provided in said writing memory cell is set at low level, a writing circuit for applying the potential of high level to said bit line connected to said writing memory cell is further provided**", does not carry any patentable weight the claim drawn to a structure, because a distinct structure is not necessarily produced.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, Adan, and Chen, and further in view of Matsumoto, US Patent No. 6,794,717 B2.

RE CLAIM 8: Adan teaches **an SOI substrate** (abstract) **in which a semiconductor substrate** (1), **an insulating layer** (2), **and a semiconductor layer** (3) **are laminated in this order, wherein said SOI substrate** (abstract) **includes a memory cell array region** (70) **formed with said plurality of memory cells** (40),

Adan shows the limitations of claim 8 as shown above. Adan is silent as to a peripheral circuit region.

However, in an analogous structure, Matsumoto teaches **a peripheral circuit region** (fig. 57 and 59, col. 29, lines 48-49) **formed with a peripheral circuit, a first element isolation film** (32, col. 29, line 53) **having a bottom face that is brought into contact with an upper surface of said insulating layer** (2) **is formed in said memory cell array region,**
and a second element isolation film (31, fig. 58, col. 29, line 40-41) **having the bottom face that is not brought into contact with the upper surface of said insulating layer** (2) **is formed in said peripheral circuit region** (col. 29, line 40-41).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ a peripheral circuit region as shown above by Matsumoto in order to form element formation regions isolated from the periphery through the complete oxide film (col. 29, lines 40-41).

RE CLAIM 9: Chang teaches (fig. 6) **a bit line** (BL) **extending along said first direction; a plurality of gate lines** (CG), **a plurality of word lines** (WL), **and a plurality of source lines** (CS), **all extending along a second direction; and a**

plurality of memory cells (40) **arranged side by side along said first direction in said element formation region** (40), **wherein said bit line** (BL) **is shared by said plurality of memory cells** (40), **and one source line** (CS) **out of said plurality of source lines** (CS) **is shared by two memory cells** (40) **which are adjacent to each other along said first direction out of said plurality of memory cells** (40).

Chang teaches substantially the limitations of claim 9 as shown above. Chang is silent as to the element isolation film.

However, in an analogous structure, Matsumoto teaches **a substrate** (1) **on which an element formation region extending along said first direction is defined by said first element isolation film** (31, abstract).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ an element isolation film as shown by Matsumoto in order to isolate the element formation regions (abstract).

RE CLAIM 10: Adan teaches a **substrate is an SOI substrate** (abstract) **in which a semiconductor substrate** (1), **an insulating film** (2), **and a semiconductor layer** (3) **are laminated in this order.**

Adan teaches limitations of claim 1 as shown above. Adan is silent as to the cell array region and a peripheral circuit region.

However, in an analogous structure, Chang teaches a **substrate has a memory cell array region** (70) **formed with said plurality of memory cells** (40).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the inventions of Chang and Adan in order to provide a nonvolatile memory array (col. 4, line 49-50) to a memory device.

Also, in an analogous structure, Matsumoto teaches **a peripheral circuit region** (fig. 57 and 59, col. 29, lines 48-49) **formed with a peripheral circuit, said first element isolation film** (32) **has a bottom face that is brought into contact with an upper surface of said insulating layer** (2)**, and a second element isolation film** (31) **having a bottom face that is not brought into contact with the upper surface of said insulating layer** (2) **is formed in said peripheral circuit region** (col. 29, line 40-41)**.**

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ a peripheral circuit region as shown above by Matsumoto in order to form element formation regions isolated from the periphery through the complete oxide film (col. 29, lines 40-41).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PETER LOXAS whose telephone number is (571)270-7380. The examiner can normally be reached on IFP.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/PETER LOXAS/
Examiner, Art Unit 2811
3/1/10

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